IN THE CLAIMS

Please amend the claims as follows:

1. (Currently Amended) A semiconductor memory integrated circuit comprising:

a semiconductor substrate;

a device isolation insulating film buried in grooves formed into said semiconductor substrate;

a cell array having an arrangement of electrically erasable and programmable nonvolatile memory cells made by stacking floating gates and control gates on said semiconductor substrate; and

a peripheral circuit disposed around said cell array on said semiconductor substrate,

at least a bottom layer of said floating gates of said nonvolatile memory cells and at least a bottom layer of gate electrodes of transistors in said peripheral circuit being formed before said device isolation insulating film is buried, then the bottom layer of said floating gates of said nonvolatile memory cells and the bottom layer of gate electrodes of transistors in said peripheral circuit being maintained in self alignment with said device isolation insulating film, N type impurities being doped into the gate electrodes of NMOS transistors and P type impurities being doped into the gate electrodes of PMOS transistors in said peripheral circuit, and

said floating gates of said nonvolatile memory cells comprise a first-layer gate electrode material film in self alignment with said device isolation insulating film and a second-layer gate electrode material film stacked on said first gate electrode material film, said control gates comprise a third-layer electrode material film, and said gate electrodes in said peripheral circuit have a three-layered structure including said first- to third-layer gate electrode material films.

2. (Previously Presented) The semiconductor memory integrated circuit according to claim 1 wherein two kinds of gate insulating transistors, thicknesses of the two kinds of gate insulating transistors being different from each other, are arranged in the peripheral circuit.

3. (Original) The semiconductor memory integrated circuit according to claim 1,

wherein different n-type impurities are doped into said floating gates of said nonvolatile memory cells and gate electrodes of NMOS transistors in said peripheral circuit, and a p-type impurity is doped into said gate electrodes of PMOS transistors in said peripheral circuit.

4. (Original) The semiconductor memory integrated circuit according to claim 1,

wherein phosphorus is doped into said floating gates of said nonvolatile memory cells.

5. (Original) The semiconductor memory integrated circuit according to claim 1,

wherein phosphorus is doped into said floating gates of said nonvolatile memory cells, and arsenic is doped into said gate electrodes of NMOS transistors in said peripheral circuit.

6. (Canceled)

7. (Cancel)

8. (Cancel)

9-20. (Canceled)

21. (Currently Amended) The semiconductor integrated memory according to claim ~~6~~ 1, wherein said first- to third-layer electrode films are in electrical contact with each other in said gate electrode of said peripheral circuit.

22. (Currently Amended) The semiconductor integrated memory according to claim ~~6~~ 1, wherein a thickness of said gate electrode comprising said first- to third-layer films is

substantially the same as a thickness of said stacked control and floating gates in said nonvolatile memory cells.

23. (Currently Amended) The semiconductor integrated memory according to claim ~~6~~ 1, wherein sidewalls of said device isolation insulating film are substantially flat.

24. (Currently Amended) The semiconductor integrated memory according to claim ~~6~~ 1, wherein a width of said device isolation insulating film from a point laterally adjacent to said bottom layer of said gate electrode and extending into said substrate is substantially uniform.

25. (Cancel)

26. (Cancel)

27. (Cancel)

28. (Cancel)